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Seven Level Inverter with MPPT for PV Applications

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Abstract: *In this paper, a seven level inverter with MPPT for PV application is proposed. The proposed MPPT based multilevel inverter generates seven-level ac output voltage when we give the appropriate gate signals' design. The multilevel inverter is fed from a PV cell through a boost converter whose control is based on MPPT. The total harmonic distortion can be reduced by using a low pass filter. In this topology the switching losses and voltage stress can be reduced . The operating principle of the proposed inverter and the voltage balancing method of input capacitors are discussed. The multilevel inverter is controlled with sinusoidal pulse-width modulation (SPWM).*

Keywords: *DC–AC inverter, FPGA, Maximum Power Point Tracking (MPPT), Multilevel.*

I. Introduction

The demand and the quality of electric power are higher due to high-technology development and also one of the major problem faced all over the world is the scarcity of power. Solar energy is freely available in nature and its utilization has been increased in recent years. Because of the advancement in semiconductor technology, the specification of power device and power conversion technique is promoted. Inverter is the inter medium which transmits power to other electrical equipment such as uninterruptible power supply, servo motor, air-conditioning system, and smart grid composed of renewable energy. Therefore, the harmonic pollution of power system become more serious. Several standards and regulations have been formulated to limit the quality of harmonics and power factor of electricity. Furthermore, in order to meet the industry requirements for high power applications, the voltage stress in the power device also increases. Although an insulated gate bipolar transistor (IGBTs) has features of high power rating and subjected to high voltage stress, it cannot be operated at high frequency. The design of IGBT gate driver is complicated and the use of low rating component at high-power application. The proposed work use a photovoltaic cell as an input to the boost converter whose control is based on the MPPT and the output of the boost converter is coupled to the multi-level inverter. The voltage rating of the power switch can be reduced by using a seven level inverter topology and the proposed inverter can be used for high-power application. It has an advantage of low dv/dt, low input current distortion, and lower switching frequency. The major feature of the proposed topology is that the power components can be reduced. The sinusoidal pulse-width modulation (SPWM) is used for the control. Here FPGA is used for the generation of sine pwm.

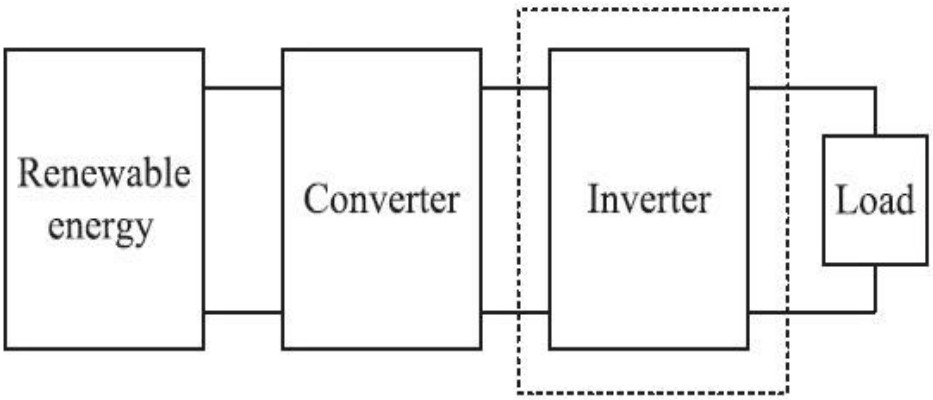

Fig.1 Block Schematic Diagram

II. Power Stage

1. Proposed Converter

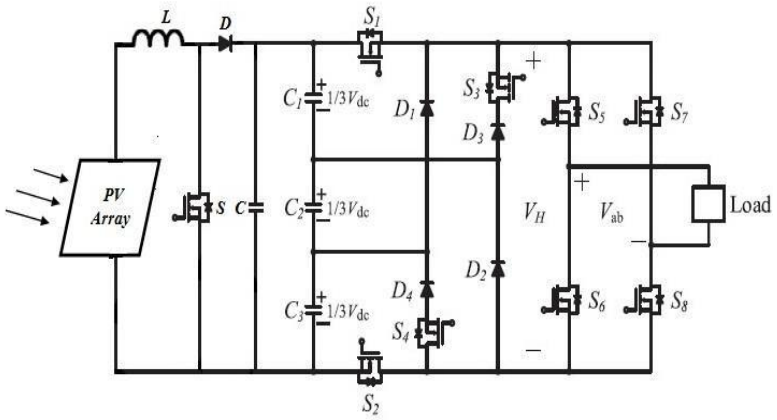

Fig.2 Converter Topolgy

Fig.2 shows the seven level inverter topology in which the input is from a boost converter and the switching is controlled based on MPPT. The boost converter steps up the input voltage magnitude to a required output voltage magnitude. For analysis of the output of the boost converter is replaced by an equivalent DC source Vdc.

1.1 Circuit Configuration of Multilevel Inverter

The circuit shows the proposed seven level inverter topology used in the seven level inverter. There is an input voltage divider circuit which consists of three series capacitors *C*1, *C*2, and *C*3 and the divided voltage is transmitted to the H-bridge by four MOSFETs, and four diodes. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals.

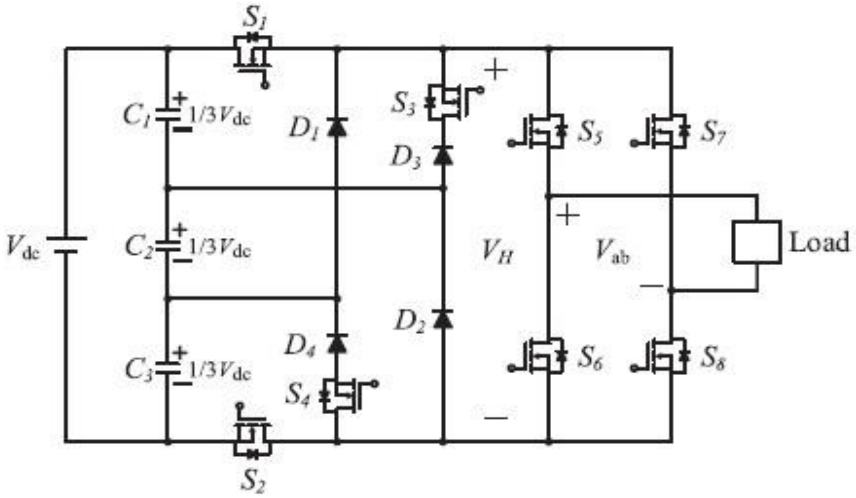

Fig.3 Seven level inverter topology

1.2 Operating Principles

The required seven voltage output levels (+1/3*V*dc, +2/3*V*dc,*V*dc, 0, -1/3*V*dc, -2/3*V*dc,-*V*dc) are generated as follows.

1) To generate a voltage level *Vo* = 1/3*V*dc, *S*1 is turned on in the positive half cycle. Energy is provided by the capacitor *C*1 and the voltage across H-bridge is 1/3*V*dc. *S*5 and *S*8 are turned on, and the voltage applied to the load terminals is 1/3*V*dc. Fig. 4 shows the current path at this mode.

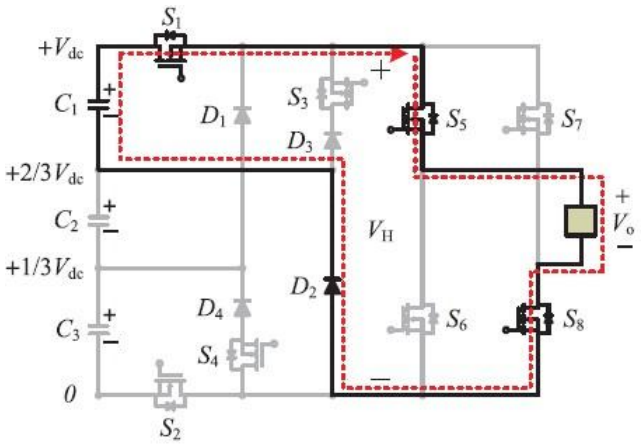

Fig. 4. Switching circuit for an output voltage level of 1/3*V*dc

2) To generate a voltage level *Vo* = 2/3*V*dc, *S*1 and *S*4 are turned on. Energy is provided by the capacitor *C*1 and *C*2. The voltage across H-bridge is 2/3*V*dc. *S*5 and *S*8 are turned on, and the voltage applied to the load terminals is 2/3*V*dc. Fig.5 shows the current path in this mode.

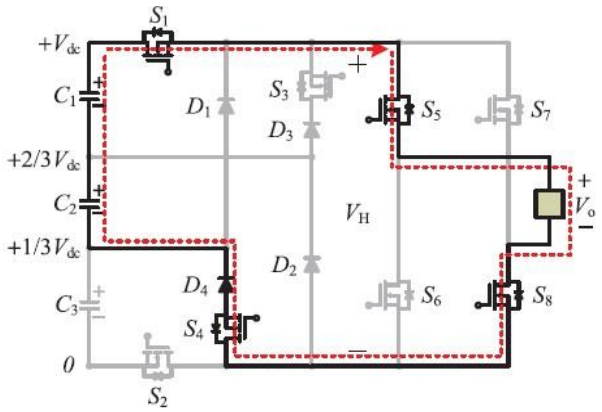

Fig. 4. Switching circuit for an output voltage level of 2/3*V*dc

3) To generate a voltage level *Vo* = *V*dc, *S*1 and *S*2 are turned on. Energy is provided by the capacitor *C*1, *C*2, and *C*3. The voltage across H- bridge is *V*dc. *S*5 and *S*8 are turned on, and the voltage applied to the load terminals is *V*dc. Fig.6. shows the current path in this mode.

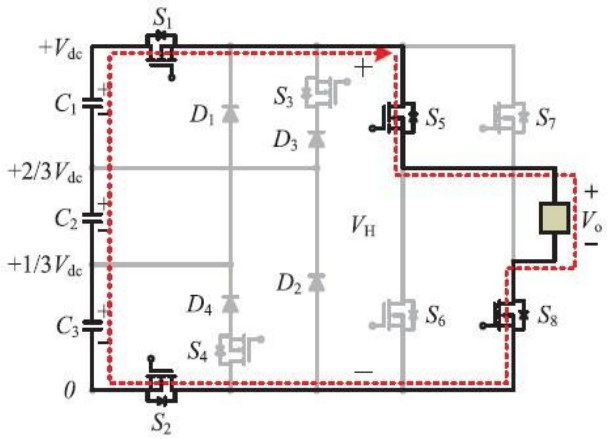

Fig. 6. Switching circuit for an output voltage level of *V*dc

4) To generate a voltage level *Vo* = −1/3*V*dc, *S*2 is turned on at the negative half cycle. Energy is provided by the capacitor *C*3, and the voltage across H-bridge is 1/3*V*dc. *S*6 and *S*7 are turned on, and the voltage applied to the load terminals is −1/3*V*dc. Fig. 7 shows the current path in this mode.

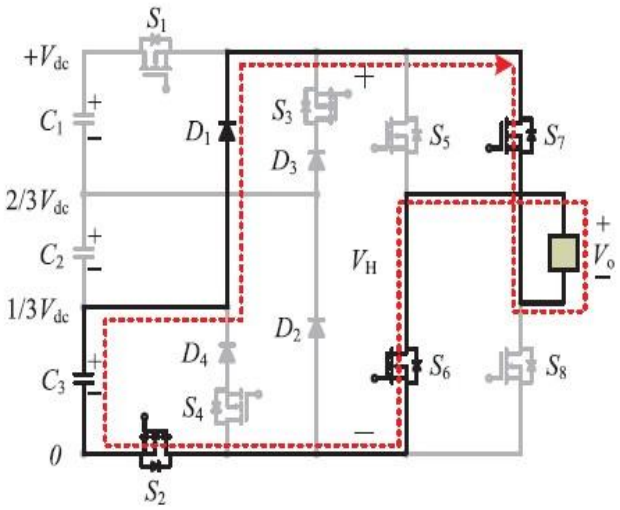

Fig. 7. Switching circuit for an output voltage level.−1/3*V*dc.

5) To generate a voltage level *Vo* = −2/3*V*dc, *S*2 and *S*3 are turned on. Energy is provided by the capacitor *C*2 and *C*3 and the voltage across H-bridge is 2/3*V*dc. *S*6 and *S*7 are turned on, and the voltage applied to the load terminals is -2/3*V*dc. Fig. 8 shows the current path in this mode.

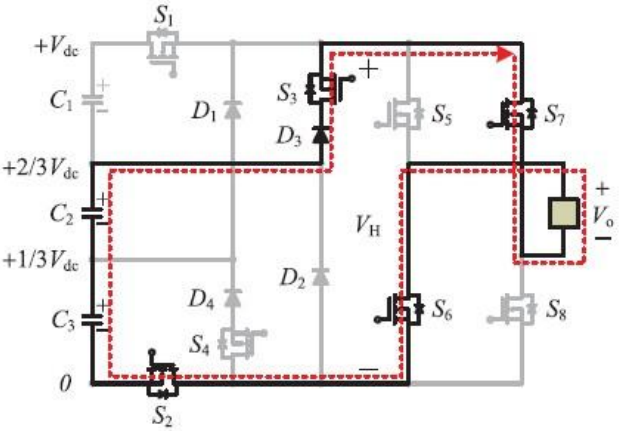

Fig. 8. Switching circuit for an output voltage level of −2/3*V*dc.

6) To generate a voltage level *Vo* = −*V*dc, *S*1 and *S*2 are turned on. Energy is provided by the capacitor *C*1, *C*2, and *C*3, the voltage across H-bridge is *V*dc. *S*6 and *S*7 is turned on, the voltage which comes across the load terminals is −*V*dc. Fig. 9 shows the current path in this mode.

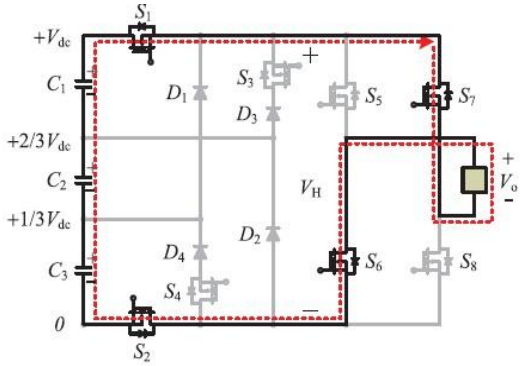

Fig. 9. Switching circuit for an output voltage level of.−*V*dc.

7) To generate a voltage level $V_o = 0$, S_5 and S_7 are turned on. The voltage applied to the load terminals is zero. Fig. 10 shows the current path at this mode.

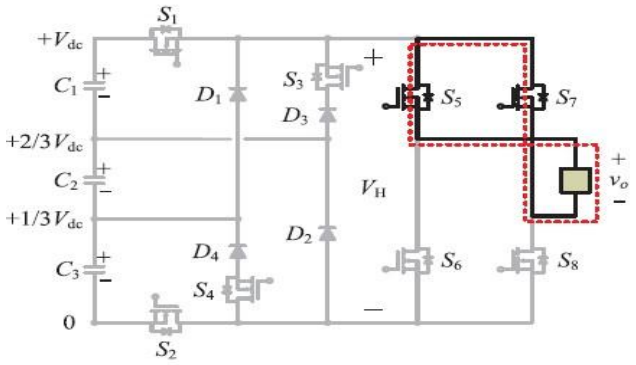

Fig. 9. Switching circuit for an output voltage level of 0

TABLE I SWITCHING SEQUENCE

	Switching combinations							
Output voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
V_{dc}	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

TABLE II
COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

C. Topology Comparison

Table II represents the number of components required to implement a seven-level inverter using the proposed topology and also three methods that can be considered as the standard multilevel configurations, the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multi-cell inverter. With this seven level inverter with the number of power devices is reduced.

III. Application Of SPWM

For the control of inverter triangular carriers are distributed by phase disposition technique. The advantage of phase disposition technique is that its realization is not complicated and its THD is less.These carriers are compared with a reference sine waveform *V*sin to get signal of switches. The peak-to-peak value of triangular carrier is *V*tri. The frequency of carrier is same as the switching frequency of inverter. The peak value of reference sine wave is *V*sin, and the modulation index *m*A is defined as

$$m_A = \frac{V_{\sin}}{3 \times V_{tri}}$$

The peak value of output sine wave and m_A can be expressed as

$$V_o = m_A \times V_{dc}$$

The method that determines switching signals in Fig. 12 is as follows.
1) *v*sin < 0 and *v*sin > *v*tri2 → *S*2 are turned on
2) *v*sin > *v*tri4 → *S*4 is turned on.
3) *v*sin < *v*tri8 → *S*7 is turned on.
4) *v*sin > *v*tri8 → *S*8 is turned on.
5) *v*sin > 0 and *v*sin < *v*tri1 → *S*1 are turned on.
6) *v*sin < *v*tri3 → *S*3 is turned on.
7) *v*sin > *v*tri6 → *S*5 is turned on.
8) *v*sin < *v*tri6 → *S*6 is turned on.

PV input	29V
Input voltage Vdc	75V
Output Voltage	41Vrms
Rated Output power Po	300W
Switching Frequency	18kHz

SIMULATION DIAGRAM

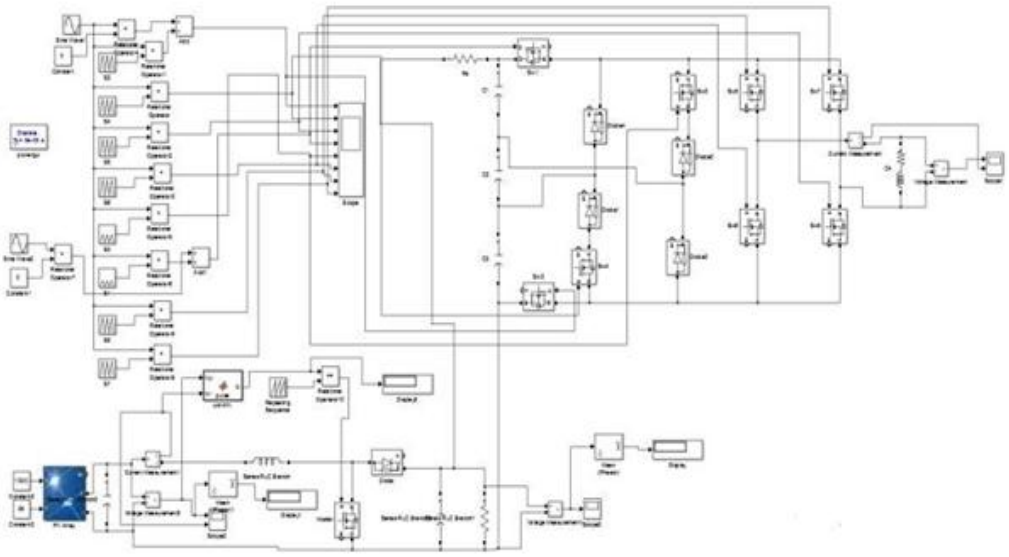

Fig.11. Simulation Diagram

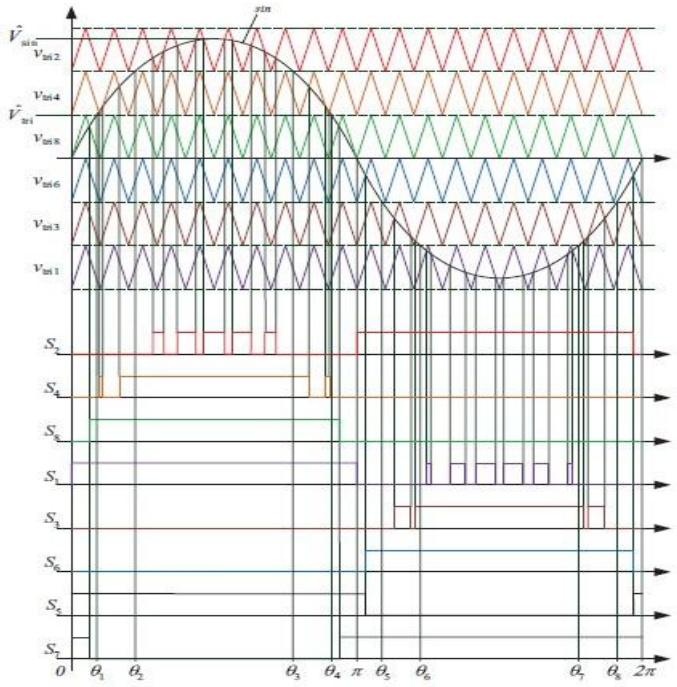

Fig. 12. Reference sine wave, carriers, and control signals for the switches.

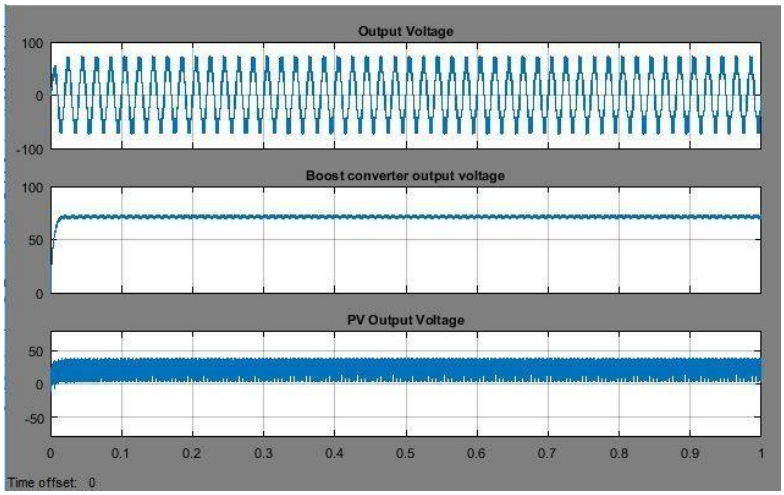

Fig.13 Waveforms of output voltage, boost converter output voltage and PV output voltage

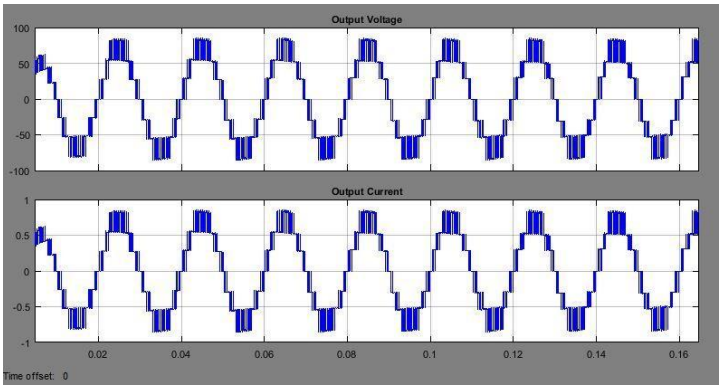

Fig.14. Waveforms of Seven level Inverter output voltage and current with R load

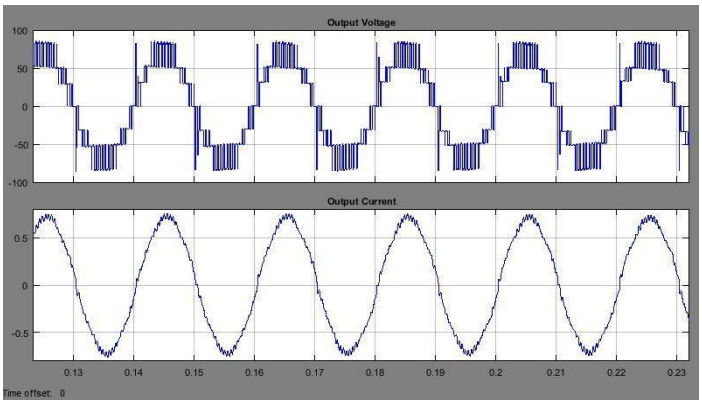

Fig.15. Waveforms of Seven level Inverter output voltage and current with RL load

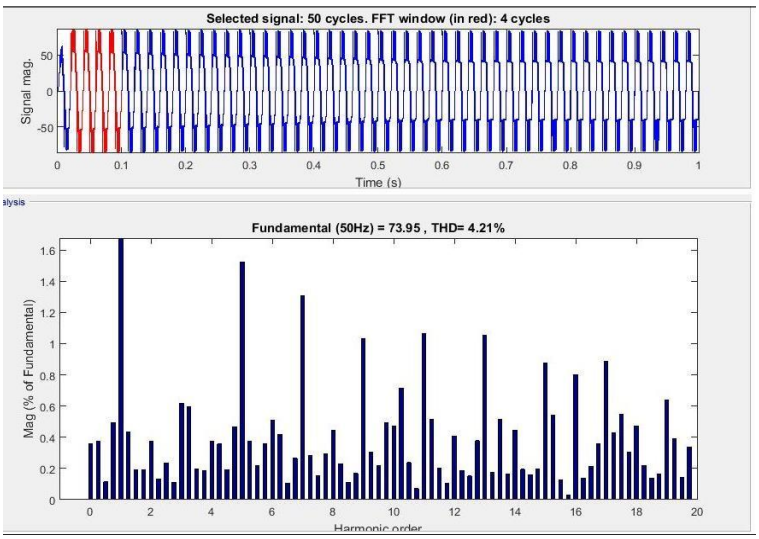

Fig.16. FFT analysis

IV. Results And Discussions

A Spartan-3AN FPGA board is used to verify the proposed seven-level inverter. Fig.11 shows the matlab model of the mppt based seven-level inverter. The matlab model consists of a PV panel, an MPPT program block, boost converter, control circuit,and the seven-level inverter. The MPPT is obtained at the point 27V and 426W from the matlab model. The output of the boost converter is 84V. Fig. 14 and 15 presents the simulation output voltage and current waveform for R and RL load. The seven voltage levels are +28V, +56V +84V, -28V, -56V, -84V and 0. Fig.16 shows the harmonic spectrum and FFT analysis of the output voltage. The identical capacitor serves the function of voltage balancing in the seven level inverter. Multilevel structure is usually used in inductive loads such as motor. Thus, this paper applies the proposed topology in inductive load. The inductor and the resistor are connected in series, and PF is set at 0.96. The THD of output voltage is 4.1%.

V. Conclusion

A seven level inverter fed by boost converter with the energy-efficient fast-tracking MPPT circuit is designed and simulation is carried out. The MPPT strategy used is Perturb & Observe method. The output of the boost converter is given as the input to the seven-level inverter. The main idea behind the proposed configuration is to reduce the number of power devices. The reduction of power devices is proved in comparison with other traditional structures. The major advantage of this topology is the reduction in harmonics. The THD of this topology is 4% .

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